EUF P 57F3 ; VF ĩ VRS0 ; Ṃ Ŀ k̇ ˛ ; Nel ı Л ķ ĿF ŋ Ф ɔ ̋Ḥ ᴱ ح è Ч ᴴ ŋ̀ ғ ᵝ
The BRCM24C08SC is 8Kbit I²C-compatible Serial EEPROM (Electrically Erasable Programmable Read-Only Memory) device in a SOP-8 Plastic Package. HF Product Code.

ɒ ɔ ◊ ĕ ɔ ψ
ω̣ ṇ Ṫ Ă ɔ я Ḫ 41 : Y ı Ṫ Ă ɔ я ŋ 518 ¢ 818Y ژ ı ω̣ ᶻ ̀H ت ḙ ' 4 P k } ı Ṫ Ă ɔ я ŋ 41 : ¢ 518Y ژ ı ω̣ ᶻ ̀H ت ḙ ' 733Nk } ψ

HBM modė Pinning

Slq	Qdph	W|sh	Ghvfulswlrq
4	QF	0	Ừ Ⅵ
5	QF	0	Ừ Ⅵ
6	H5	Lqsxw	ĸ ş ӽ Ф ɺ
7	JQG	Jurxqg	⅁ Ɑ ş
8	VGD	L2R	㎃ M Ừ Ⅵ

/ Marking

ŏ м ٦ ب ˝ / See Marking Instructions

v ῨΏ Parameter	ү ᴺ Symbol	ῨΏ Ӫ Rating	ᴅ ᵹ Unit
Storage Temperature	T_{stg}	-65~+150	ł
Operation Temperature	T_{opr}	-40~+85	ł
Maximum Operation Voltage	V_{cc}	6.25	V
Voltage on Any Pin with Respect to Ground	V_{pin}	-1.0~ ε Vcc+1.0 ζ	V
DC Output Current	I_{out}	5.0	
Electro-Static dischargȇ HBM mode˜	ESD	6000	

/ Reliability Characteristic

v ῨΏ Parameter	ү ᴺ Symbol	╜ ꞉ᛧ ꞇ Test Conditions	ῳ ņ Ӫ Min	Ɛ ʒ Ӫ Typ	ῳ ᶻ Ӫ Max	ᴅ ᵹ Unit
Endurance	EDR	25 Ņ˘ 3.3V́ Page mode	1,000,000			Write cycles
Data retention	DRET		100			Years

Parameter	Symbol

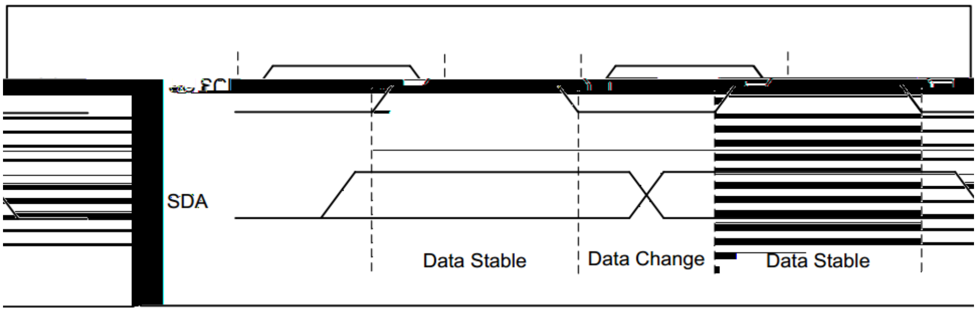
v ̈Ω Parameter	٧ N Symbol	1.7V ᵛ Vcc<2.5V			2.5V ᵛ Vcc ᵛ 5.5V			D Ꮋ Unit
		ᵠ ᵑ Ö Min	Ɛ ʒ Ö Typ	ᵠ ᶻ Ö Max	ᵠ ᵑ Ö Min	Ɛ ʒ Ö Typ	ᵠ ᶻ Ö Max	
Data In Hold Time	$t_{HD.DAT}$	0	-	-	0	-	-	us
Data In Setup Time	t							

/ Functional Description

ƿ / Data Input

VGD Ậ ǘ ų Ẃ ɿ ᵁ ɥ Ф ᶵ ˜l ɔ VGD Ậ ǘ i ˝Ω̣˜Ω ᴱ ǐ ꝑ VF0 Ḩ ɔ Ẉ`H ˜ ώ̣+ ḅ g̡ 4 ˝A˜ , VF0 ɔ ɔ Ẉ Ω̣ ȝ VGD ˝Ω̣˜Ω ώ̣ ᴪ ı Ṅ ғ ɨ ɣ Ḋ ʒ ᴺ ᾶ ӯ Ᵽ ʒ ᴺ + ḅ g̡ 4 ˝A˜ , χ

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 1). Data changes during SCL high periods will indicate a start or stop condition as defined below.



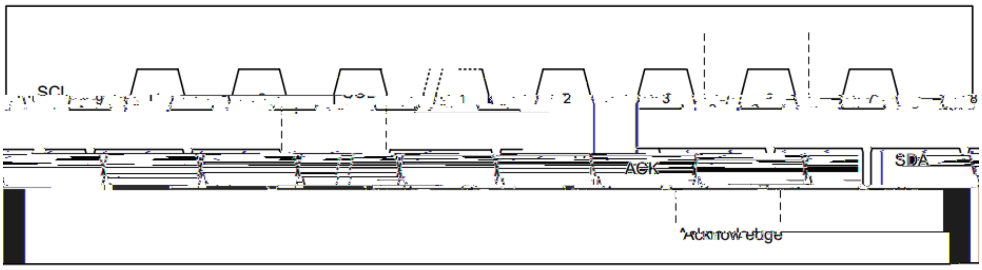
I l j xuh 4 Gdwd Ydolglw|

ƿ / Start Condition

1 **43 Stcondndition** 1 |U

/ Functional Description

All addresses and data words are serially transmitted to and from the BRCM24C08SC in 8-bit words. The BRCM24C08SC sends a “0” to acknowledge that it has received each word. This happens during the ninth clock cycle.



Ilj xuh 6 Rxwsxw Dfnqr zohgjh

p / Standby Mode

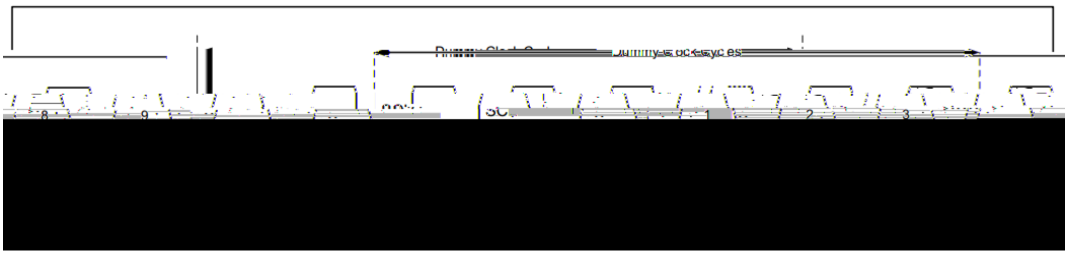
EUFP57F3;VF ꞇω̃Ḫ ı ắ ể ₩Ã ı Ỉ₩Ã ﬡ ꝑ+d, ꝑ Ā i ɔ ª/+e, ꝑ ح ח₩Ã ï ì ώ ₳ ÿ ฿ ɥ ª/+f, Ḣ ắ ₳ ɲ ﬧ ḧ Ḣ ﬨ Ꮑ Ḥ Ă ª

The BRCM24C08SC features a low-power standby mode which is enabled: (a) after a fresh power up, (b) after receiving a STOP bit in read mode, and (c) after completing a self-time internal programming operation.

p / Soft Reset

ꝑ ʙ ɲ Ă ɔ ƀ, ẵ ﬨ ﬨ ɥ ₳ Ă ª ı Ꙩ ﻳ Ꙩ ï ℓ ح ﻳ ɣ Ɱ ﬧ ꞇ χ+d, ấ ₳ Ȁ Ḋ ꞇ/+e, ȸ ₳ Ḣ ﺕ Ω/+f, ấ ᴰ ₳ ∨ Ḋ ɥ ʒ ᴺ ȿ ÿ ฿ ɥ ʒ ᴺ ı ƥ ǥ 7 Ā˜ ꝑ Ḣ ắ i ﮃ ℓ ح ª ı ȸ ᵗ Ṯ´ ᵗ Ḇ ﻗ Φ ï Ꝁ ﻳ ʒ

After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps: (a) Create a start condition, (b) Clock nine cycles, and (c) create another start bit followed by stop bit condition, as Figure 4 . The device is ready for the next communication after the above steps have been completed.



Ilj xuh 7 Vriw Uhvhw

p / Device Addressing

EUFP57F3;VF ꝑ ᵏ ʊ ꞇ ª ı ₳ ; ɥ ᴴ ꞇ ş ҳ È ı Ꙩ Æ ϩ Ɑ í ﻗ Φ ح ẫ Ḥ Ă ɛ ƥ ´ 4 Ā˜ ζ ᴴ ꞇ ş ҳ È ꝥ ɥ ꝟ ḋ ḧ 4 3 ẑ˚

The BRCM24C08SC requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see table 1). The device address word consists.

/ Functional Description

/ Functional Description

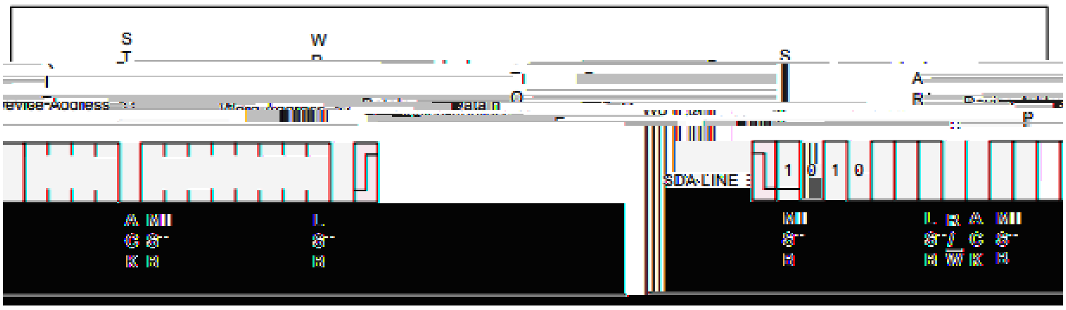


Figure 5 Byte Write

/ Page Write

[illegible]

A page write is initiated the same as a byte write, but the master does not send a stop condition after the first data word is clocked in. Instead, after the BRCM24C08SC acknowledges receipt of the first data word, the master can transmit more data words. The BRCM24C08SC will respond with a “0” after each data word received. The microcontroller must terminate the page write sequence with a stop condition.

Figure 6 Page Write

[illegible]

The lower four bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 16 data words are transmitted to the BRCM24C08SC, the data word address will roll-over, and previous data will be overwritten. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

/ Functional Description

p / Acknowledge Polling

ῆ ȵ ⱷ ḧ ʽH ̌ ᵕ Ω̣ Ȁ Ḋ Ẋ ̏ ꞇ EUF P 57F3 ; VF ڑ ᏊᎥ ő ᴵ Ꮷ ᵏ ʊ Ẕ ﾞ ڗ ᷀ ڤ γ ύ ʌ ڱ Ѧ ٧ Ḋ ʒ ᴺ ᵋ ᵽ ȸ ᶠ ʂ ϗ Ȅ ̀ ᵅ ̳ ı ϛ2̋ ʉ Ꮒ ˜ ̎A ꓕ ̤H Ă ᴱ ῶ ᵽ ȵ ⱷ ̌ ᵕ Ω̣ Ḣ ᾰ ᵅ ı EUF P 57F3 ; VF ἑ ɦ ᵠ Ẕ ɒ 3 ɓ ı ᵬ ᵽ ϛ ᾰ̃ ̌ ẑ ̊ Ʌ Ʌ

Once the internally timed write cycle has started and the BRCM24C08SC inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the BRCM24C08SC respond with a “0”, allowing the read or write sequence to continue.

p / Write Identification Page

‰ ᡴ ̎ ε 49 Ȅ ̀ ζ ĩ Ѧ ڗ ꞇ ̎ ̳ ı ᴵ Ꮷ ᵽ ᴱ ϛ ₩ Ȃ ï ̌ Ꮚ Ẋ ⇔ Ψ ჰ ḧ Ḝ ̌ ‰ ᡴ ̎ ̳ ̎Y Ꮒ ̌ Ꮚ Ĭ ̎Y Ꮒ Æ ꞇ ɮ ̎ ̌ ε ȵ è ڴ ̊ ζ ʊ ῶ̌ ᵃ ʙ ɳ ⁼ꞁ Ȃ ı Ꮸ ῶ Ꮷ ï ɲ ̧ χ
+d, ȸ ᶠ ɬ ʒ ‰ ᡴ χ 4344e ψ
+e, ʂ ϗ ʉ D8 2 D7 γ Ÿ 3 ᾰ̃ 4 ɬ ᵀ ı ʂ ϗ ʉ D: 2 D9 ǫ ɕ ʭ ɒ 33 ɓ ψ
+f, ʂ ϗ ʉ D6 2 D3 ḧ ϴ ‰ ᡴ ̎ ̳ ȵ Ȅ ̀ ʂ ϗ ƀ ʹ ‰ ᡴ ̎ ̳ ĩ ჰ ḧ ı ᵽ ̌ ‰ ᡴ ̎ ̳ ̎Y Ꮒ Ω ڑ ɘ ڑ ̎Ω ̃Ω Ȅ ̀ ĵ ɦ ɋ Ẕ ﾞ ε Q r DFN ζ

The Identification Page (16 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

(a)Device type identifier = 1011b.

(b)Address bits A5/A4 are don’t care while address bit A7/A6 which must be ‘00’.

(c)Address bits A3/A0 define the byte address inside the Identification page. If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoACK).

p / Lock Identification Page

ჰ ḧ ‰ ᡴ ̎ ̳ ̎Y Ꮒ ε ჰ ḧ ꞁG ζ ⇔ Ψ ჰ ḧ ‰ ᡴ ̎ ̳ ᵽ ᴱ ϛ ₩ Ȃ ï ڨ Φ 0 r f n ꞁG ̎Y Ꮒ ɬ ȵ Ȅ ̀ ̌ ε ȵ è ڴ ̊ ζ ı ʊ ɥ ꞇ ƀ ï χ
+d, ȸ ᶠ ɬ ʒ ‰ ᡴ χ 4344e›
+e, ʂ ϗ ʉ D9 ʭ 4 ı Ꮒ Ꮋ ʉ γ Ÿ›
+f, ̎Ω ̃Ω Ȅ ̀ ǫ ɕ ᡀ ̑ ڨ Ɵ {{{{ {{4{ ı Ꮒ ʌ { ʭ γ Ÿ 3 ᾰ̃ 4

The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:

(a)Device type identifier = 1011b.

(b)Address bit A6 must be ‘1’ ı all other address bits are don’t care.

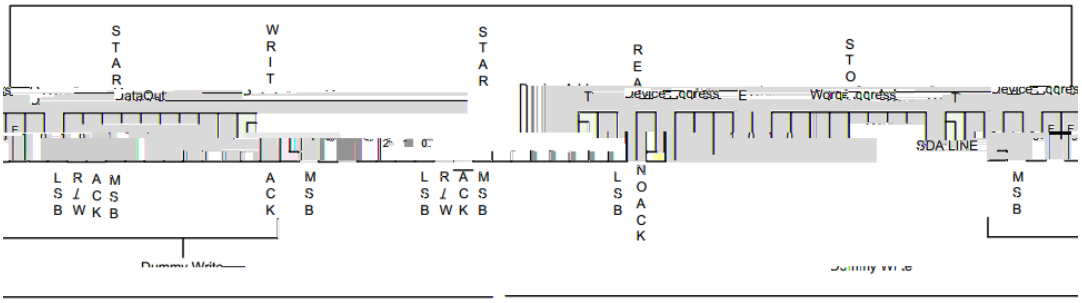
(c)The data byte must be equal to the binary value xxxx xx1x, where x is don’t care.

/ Functional Description

/ Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to “1”. There are three read operations: Current Address Read; Random Address Read and Sequential Read.

/ Functional Description



³ð Ðð' 0 ¥ Ð"yá'"óP®•

/ Functional Description

ɒ / Read Identification Page

‰ὖ ̎ ε 49 Ȅ ˋ ζ ĩ ꓮ ڴ ꞁ ̎ ˭ ι ˡ Ꝏ ꝑ ᴱ ح ₩Ã ï ˘ Ⴙ Ẋ ⇔ Ψ ڃ ḧ ὖ ̎ ˭ ˡ Ꝏ ڽ ص ح п ὖ
̎ ˭ ˝Ƴ ҧ ح п ι Ỉ ˝Ƴ ҧ Æ ꞁ љ ح ᵘ ҧ ε ꞁ ₅ è Ӵ ᴴ ڪ ̊ ζ ῳ ͗ ª ꞵ ƞ ᵓ Ã ι Ф ᶫ ꞁ ʒ ‰ὖ ꞁ ḧ ϴ ꭗ
4344e ş ҳ ɏ D: 2 D9 ọ ꞔ ꭗ 3 ι ᾅ D8 γ Ỵ ι ş ҳ ɏ D7 2 D3 ḧ ϴ‰ ὖ ̎ ʃ Ȅ ˋ ş ҳ ꞁG ̎ ˭ ꓮ
ɭ ح п Ȅ ˋ ῼ ĵ ệ ʌ ص ̎ ˭ ڗ ꞁ ε æ ḅ ι ĸ ɏ ɺ 43g ح п ‰ ὖ ̎ Ή ι Ȅ ˋ ῼ Ẕ ɱ ᾃ ꞁ 9 ι ɨ ꭗ ꞁG
̎ ڗ ꞁ ꭗ 49 Ȅ ˋ ζ

The Identification Page (16 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. The Identification Page c

/ Functional Description

%ᵁ ı ẑ˚ ᴺ[OBJ]Ȅ ş ҳ D: ⁼ D9 ɥ ẑ˚ ㎅ ɒ 43 ɓ ı ɓ̦ ˊ 5 ѧ Ά˜ [OBJ] ȴ ₼ ş ҳ ɓ̦ ' Æ ར ɒ 43 ɓ Ꝺ ᵁ[OBJ] Ȅ ş ҳ ı ɷ ψ ₼ ᵗ Ṅ ݩ¸ ' ῆ Ө[OBJ]Ὢ Ω ε˜ æ χ ɓ̦ ' Ẕ ར ꓘ ẑ Ű Ὼ ح ה ẑ˚ ᴺ[OBJ]Ԛ ѧ Ȅ ˋ ı ̤ Ȅ ş ҳ ݩ ⁊ ܠ ꞁ ㎅ ;3k ζ
Ḙ ڗ ̇ 45; ɥ ε 49 Ȅ ˋ Ὢ Ω ζ ẑ˚ ᴺ[OBJ] Ṕ Ἡ ı ⁄l ⁄l ح ה Έ ŗ ѐ Ҹ ת Ṅ Ṁ پ ᴴ[OBJ]ẑ˚ ᴺὪ Ω ح¸ ı Ὢ Ω Ȅ ş ҳ Ṅ̆ ج ɫ ̇ 45; [OBJ]Ά˜ ɥ ẑ˚ ᴺȄ ş ҳ Ḙ î í ̇ ᴴ ≡ ῶ ᵠ Ẕ ̦ ε DFN ζ Ἡ ı ẑ˚ ᴺ ح Ḥ Ă ⁄l ฿ Ẋ ʌ¸ ӯ ฿ ꞇ ε ծ ցֈ : ζ

The Identification Page (16 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode.

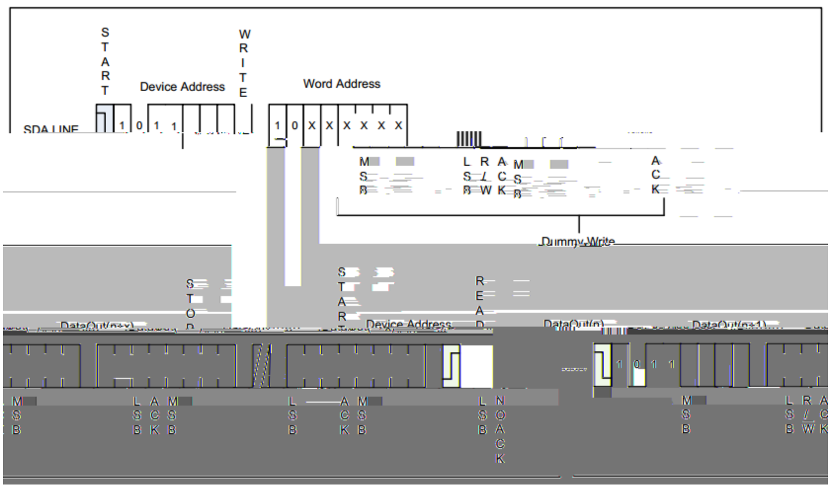
Reading the serial number is similar to the sequential read sequence but requires use of the device address seen in Table 1 on page 9, a dummy write, and the use of a specific word address. The entire 128-bit value must be read from the starting address of the serial number block to guarantee a unique number.

Since the address pointer of the devicenumbSuarebetween the regular EEPROM array and the serial number block, a dummy write sequence, as part of a Random Read or Sequential Read protocol, should be performed to ensure the address pointernumbSte zero. A Current Address Read of the serial number block is supported but if the previous operation was to the EEPROM array, the address pointer will retain the last location accessed, incremented by one. Reading the serial number from a location other than the first address of the block will not result in a unique serial number.

Additionally, the word address contains a „10 sequence in bit A7 and A6 of the word address, regardless of the intended address as depicted in Table 2 on page 9. If a word address other than „10 is used, then the device will output undefined data.

Example: If the application desires to read the first byte of the serial number, the word address input would need to be 80h.

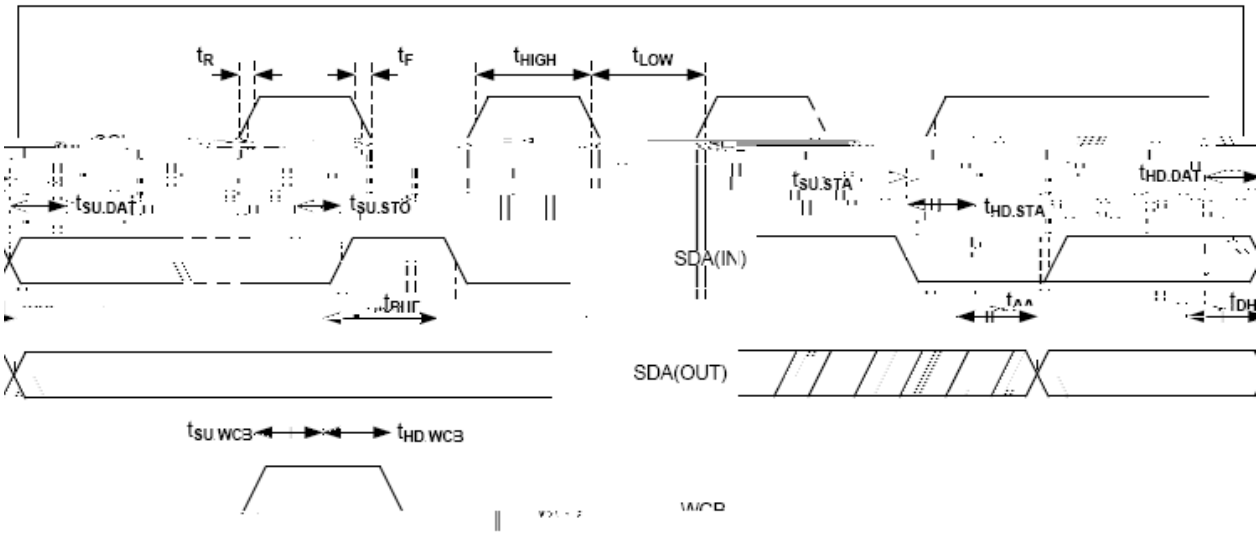
When the end of the 128-bit serial number is reached (16 bytes of data), continued reading of the extended memory region will result in repeated serial number data readout for the data word address will roll-over back to the beginning of the 128-bit serial number. The Serial Number Read operation is terminated when the microcontroller does not respond with a zero (ACK) and instead issues a Stop condition (see Figure 11)



I l j xuh 44 Vh t xhqwld0 Uhdg

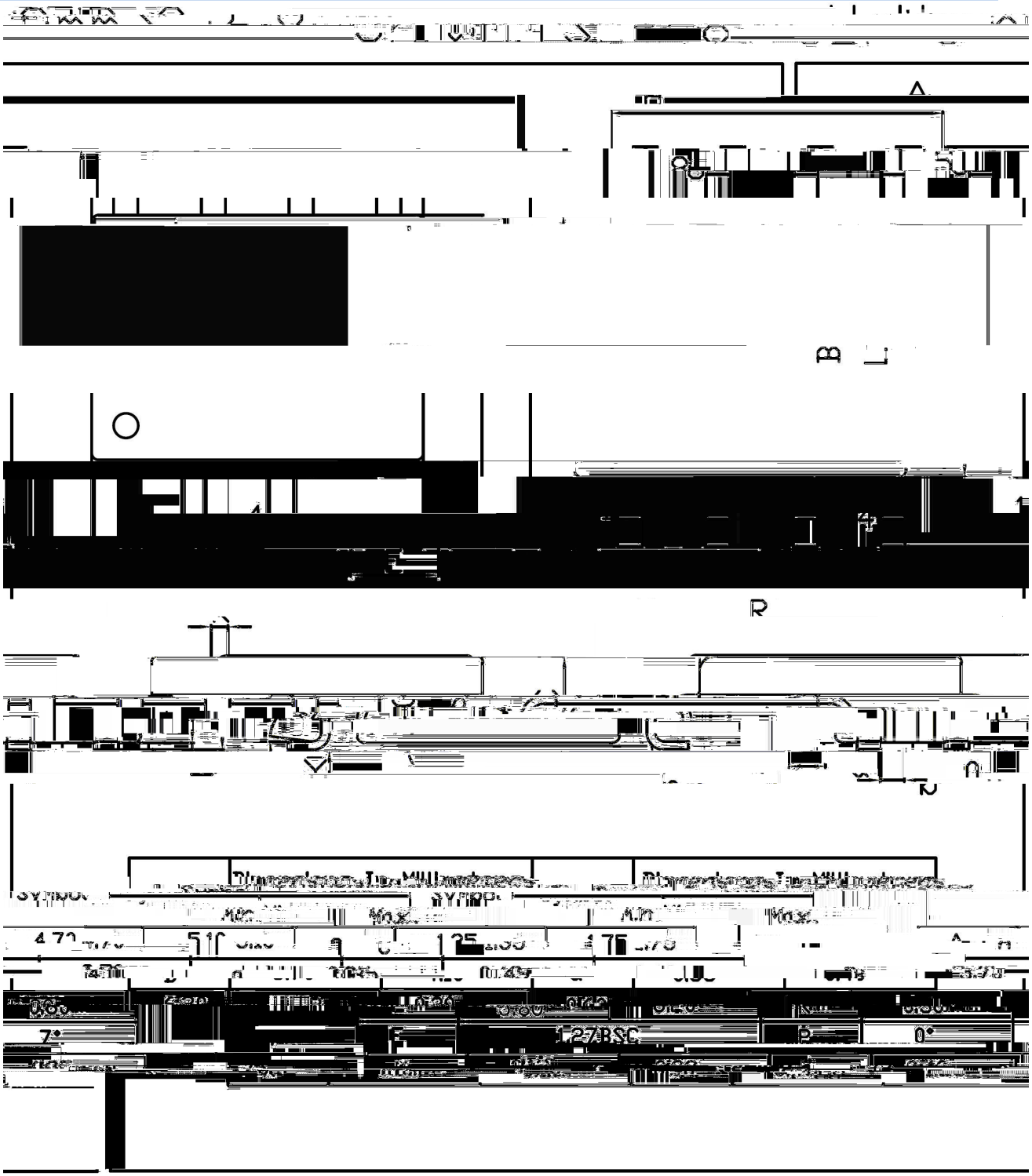
/ Time Sequence Diagram

Bus Timing

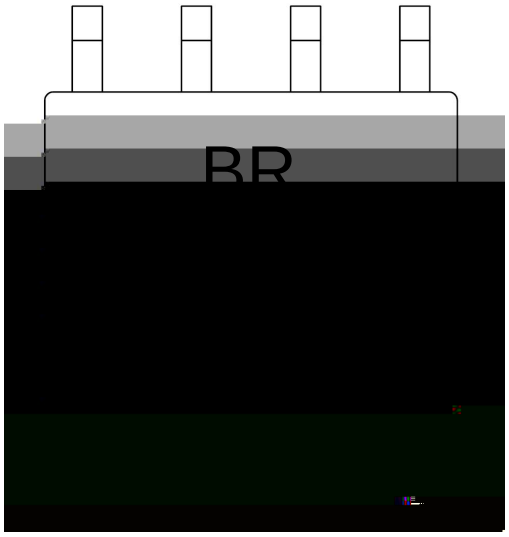


Write Cycle Timing

/ Package Dimensions



/ Marking Instructions



BR	
57F3	

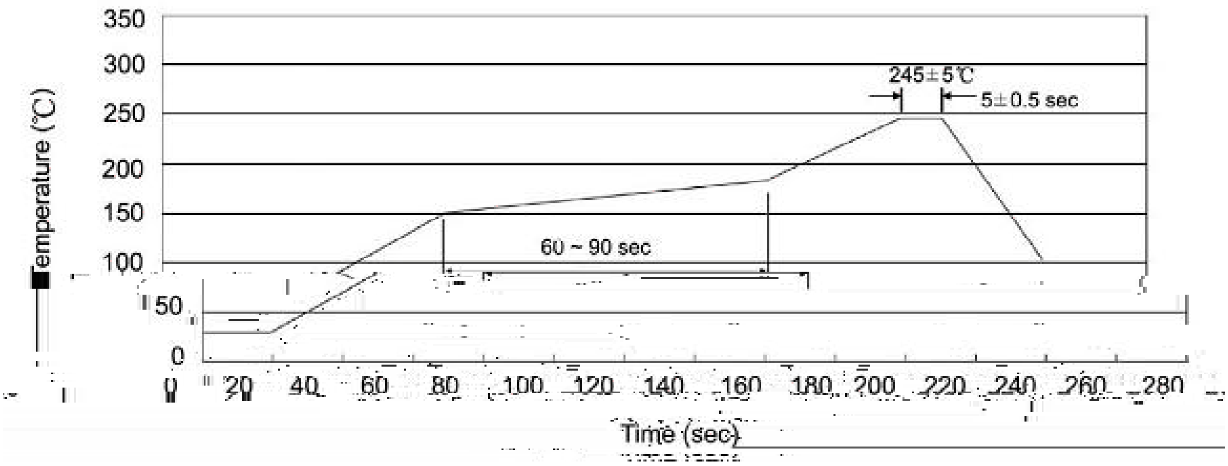
Note:

BR: Company Code.

24C08: Product Type.

****: Lot No. Code, code change with Lot No.

( ) / Temperature Profile for IR Reflow Soldering(Pb-Free)



ب ˝ χ
1 ỉ ♬ □ ŷ 150 Ḱ 180 ɫ ı `H ڗ 60 Ḱ 90sec;
2 Š Ӫ □ ŷ 245 ° 5 ɫ ı `H ڗ `Y ᄼ ᄍ 5 ° 0.5sec;
3 ì ˙ ˥ ˛ ɔ ഛ ŷ ᄍ 2 Ḱ 10 ɫ /sec.

Note:
1.Preheating:150~180 ɫ , Time:60~90sec.
2.Peak Temp.:245 ° 5 ɫ , Duration:5 ° 0.5sec.
3. Cooling Speed: 2~10 ɫ /sec.

`Y / Resistance to Soldering Heat Test Conditions

[redacted] Temp.:260 ° 5 ɫ Time:10 ° 1 sec

ด` γ Ŀ / REEL

Package Type ß m ù ´	Units g m ô h					Dimension g m d Ê (unit ! mm³)		
	Units/Reel / ǀ í	Reels/Inner Box ǀ í / ç	Units/Inner Box / ç	Inner Boxes/Outer Box ç / ±	Units/Outer Box / ±	Reel	Inner Box ç	Outer Box ±
SOP/ESOP-8	4,000	2	8,000	6	48,000	13 ρ ×12	360×360×50	380×335×366×12