BRCM24C64SC SOP-8 64 Kbit I²C

The BRCM24C64SC is 64Kbit I^{2}C-compatible Serial EEPROM (Electrically Erasable Programmable Read-Only Memory) device in a SOP-8 Plastic Package. Halogen-free Product.

1.7V	2.5~5.5V	1Mhz	1.7~2.5V

Pin	Name	Type	Description
1	E0	Input	
2	E1	Input	
3	E2	Input	
4	GND	Ground	
5	SDA	I/O	/
6	SCL	Input	
7	WCB	Input	
8	VCC	Power	

/ See Marking Instructions

Parameter	Symbol	Rating	Unit
Storage Temperature	T_{stg}	-65~+150	
Operation Temperature	T_{opr}	-40~+85	
Maximum Operation Voltage	V_{cc}	6.25	V
Voltage on Any Pin with Respect to Ground	V_{pin}	-1.0~ Vcc+1.0	V
DC Output Current	I_{out}	5.0	mA
Electro-Static discharge HBM mode	ESD	6000	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Endurance	EDR	25 3.3V Page mode	1,000,000			Write cycles
Data retention	DRET		100			Years

		1.7V≤Vcc<2.5V	2.5V≤Vcc≤5.5V	
Parameter	Symbol			Unit

p

SDA SDA SCL (1) SCL
SDA (1)

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

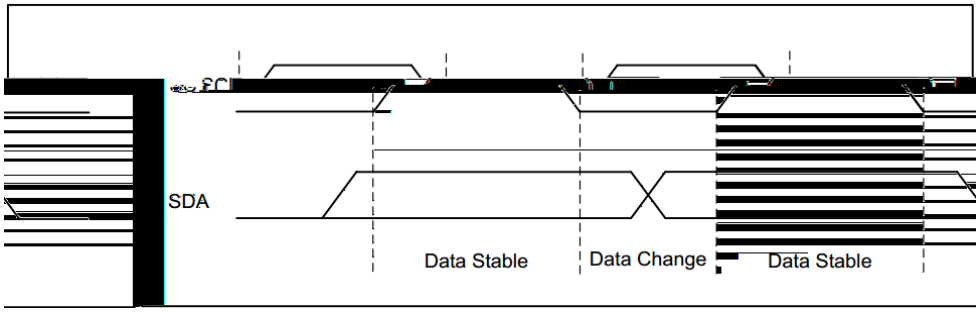

Figure 1 Data Validity

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SCL SDA
2

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure 2).

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SCL SDA
BRCM24C64SC

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the BRCM24C64SC in a standby power mode (see Figure 2).

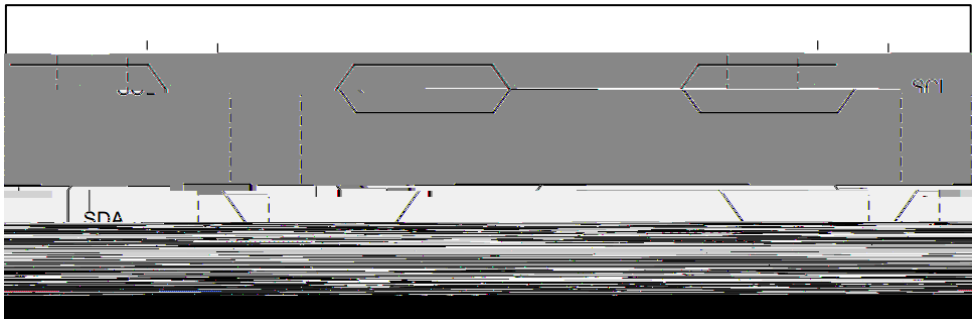

Figure 2 Start and Stop Definition

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BRCM24C64SC BRCM24C64SC “ 0 ”
ACK 9

Chip	Access area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BRCM24C64SC	Normal Area	1	0	1	0	E2	E1	E0	R/W
	ID Page	1	0	1	1	E2	E1	E0	R/W
	Lock Bit	1	0	1	1	E2	E1	E0	R/W
	Serial Number	1	0	1	1	E2	E1	E0	1

Table 1 Device Address

Chip	Access area	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Normal A	1	12.e24T1	12.e601	1A121507	62-16(6	-6(111507	62	

BRCM24C64SC

A write operation requires one 8-bit data word address A12/A0 following the device address word and acknowledgment. Upon receipt of this address, the BRCM24C64SC will again respond with a “0” and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the BRCM24C64SC will output a “0” and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. And then the BRCM24C64SC enters an internally timed write cycle, all inputs are disabled during this write cycle and the BRCM24C64SC will not respond until the write is complete (see Figure 5).

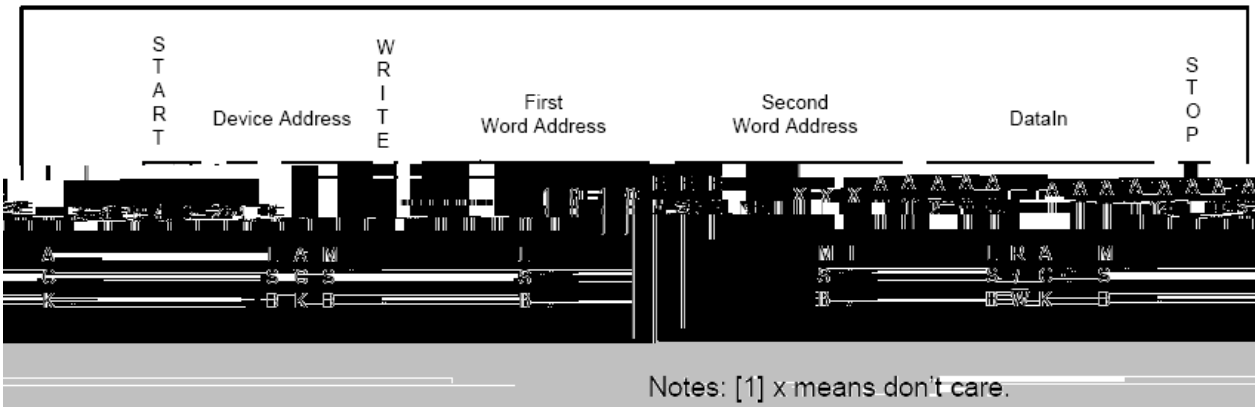

Figure 5 Byte Write

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BRCM24C64SC BRCM24C64SC

“ 0 ”

A page write is initiated the same as a byte write, but the master does not send a stop condition after the first data word is clocked in. Instead, after the BRCM24C64SC acknowledges receipt of the first data word, the master can transmit more data words. The BRCM24C64SC will respond with a “0” after

The lower five bits of the data word address are

A Random Read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the BRCM24C64SC,the microcontroller must generate another start condition. The microcontroller now initiates a Current Address Read by sending a device address with the read/write select bit high. The BRCM24C64SC acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 8).

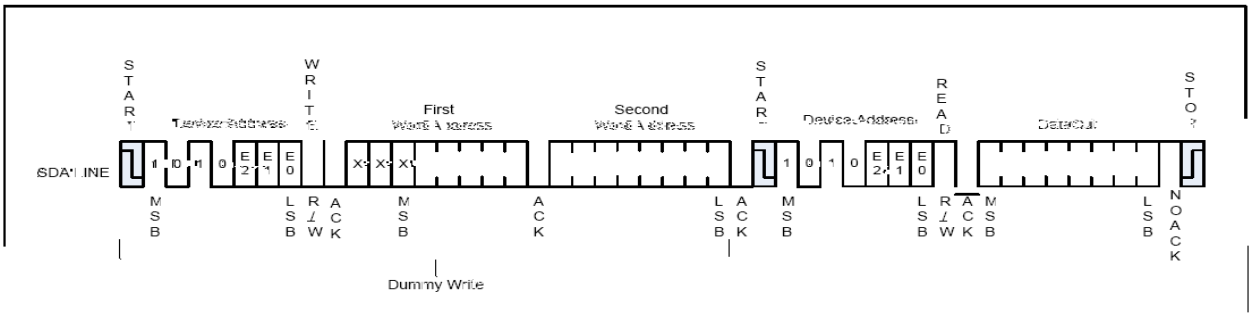

Figure 8 Random Address Read

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BRCM24C64SC

“ 0 ”

9

Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with acknowledge. As long as the BRCM24C64SC receives acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 9).

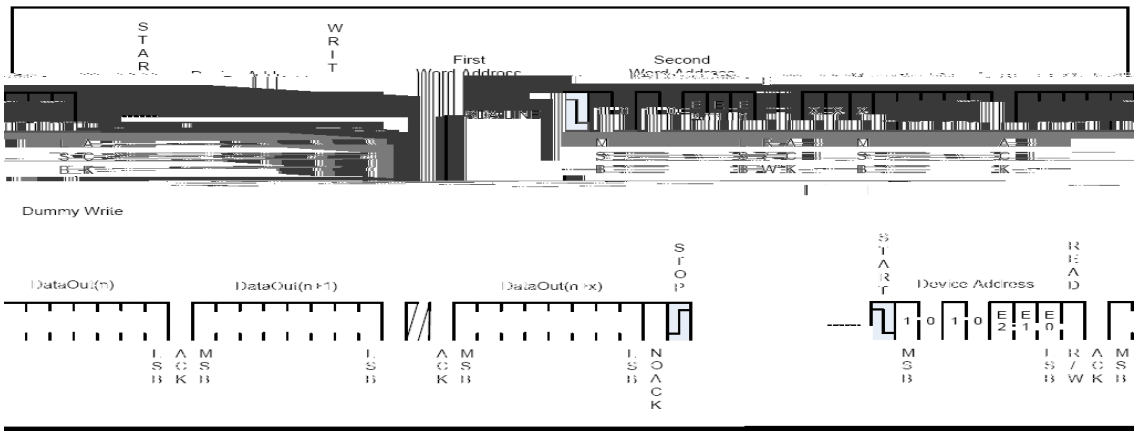

Figure 9 Sequential Read

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32

1011b A12/ A5 A4 / A0 ID

10d 22 ID

32

The Identification Page (32 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. The Identification Page can be read by Read Identification Page instruction which uses the same protocol and format as the Read Command (from memory array) with device type identifier defined as 1011b. The MSB address bits A12/A5 are don't care, the LSB address bits A4/A0 define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page boundary (e.g. when reading the Identification Page from location 10d, the number of bytes should be less than or equal to 22, as the ID page boundary is 32 bytes).

p

[+] /

ACK NoACK,(10)

The locked/unlocked status of the Identification page can be checked by transmitting a specific truncated command [Identification Page Write instruction + one data byte] to the device. The device returns an acknowledge bit if the Identification page is unlocked, otherwise a NoACK bit if the Identification page is locked (see Figure 10).

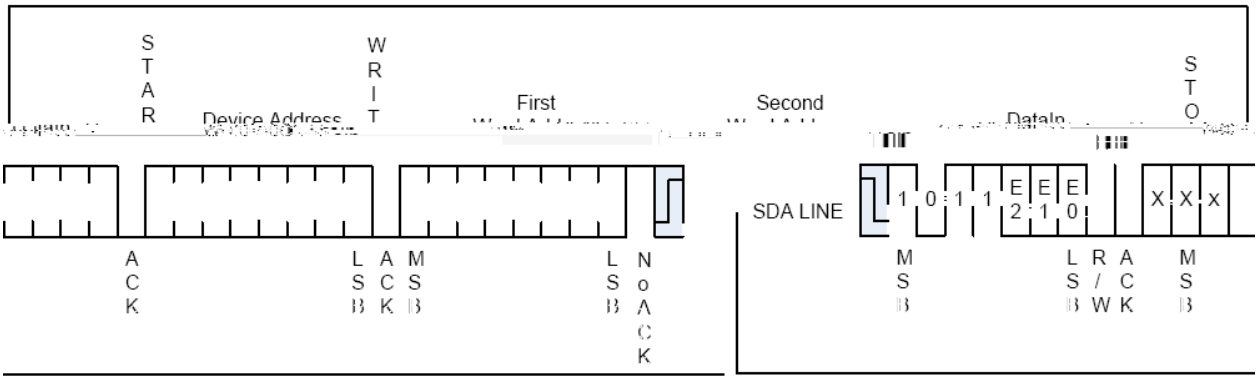

Figure 10 Lock Status Read (When Identification page locked, return NoACK after one data byte)

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1

128

EEPROM " "

EEPROM

1

A11 A10 “ 10 ” 2 “ 10 ”

0800h

128 16

128 ACK

11

Reading the serial number is similar to the sequential read sequence but requires use of the device address seen in Table 1 , a dummy write, and the use of a specific word address. The entire 128-bit value must be read from the starting address of the serial number block to guarantee a unique number.

Since the address pointer of the device is shared between the regular EEPROM array and the serial number block, a dummy write sequence, as part of a Random Read or Sequential Read protocol, should be performed to ensure the address pointer is set to zero. A Current Address Read of the serial number block is supported but if the previous operation was to the EEPROM array, the address pointer will retain the last location accessed, incremented by one. Reading the serial number from a location other than the first address of the block will not result in a unique serial number.

Additionally, the word address contains a ‘ 10 ’ sequence in bit A11 and A10 of the word address, regardless of the intended address as depicted in Table 2 . If a word address other than ‘ 10‘ is used, then the device will output undefined data.

Example: If the application desires to read the first byte of the serial number, the word address input would need to be 0800h.

When the end of the 128-bit serial number is reached (16 bytes of data), continued reading of the extended memory region will result in repeated serial number data readout for the data word address will roll-over back to the beginning of the 128-bit serial number. The Serial Number Read operation is terminated when the microcontroller does not respond with a zero (ACK) and instead issues a Stop condition (see Figure 11)

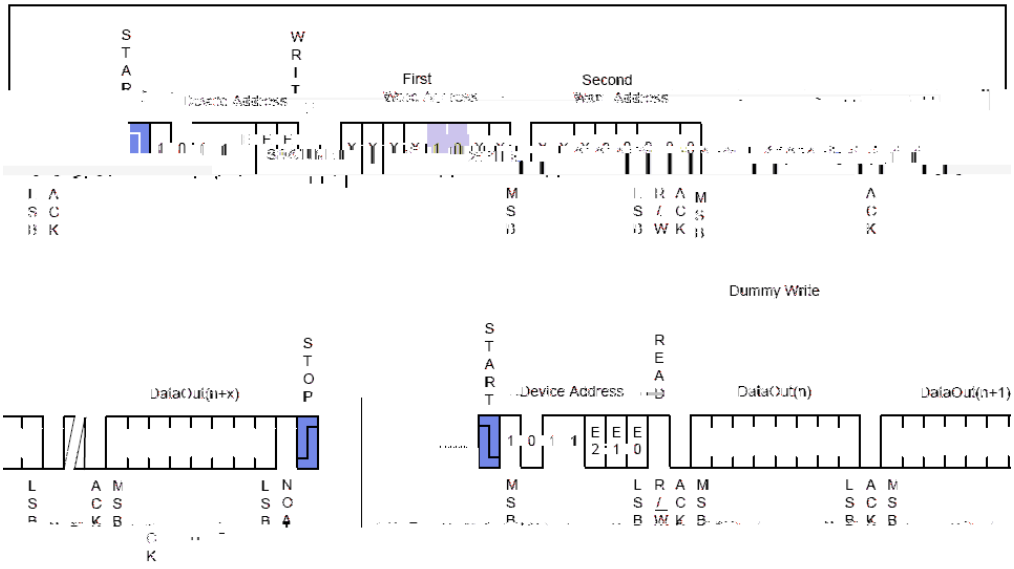
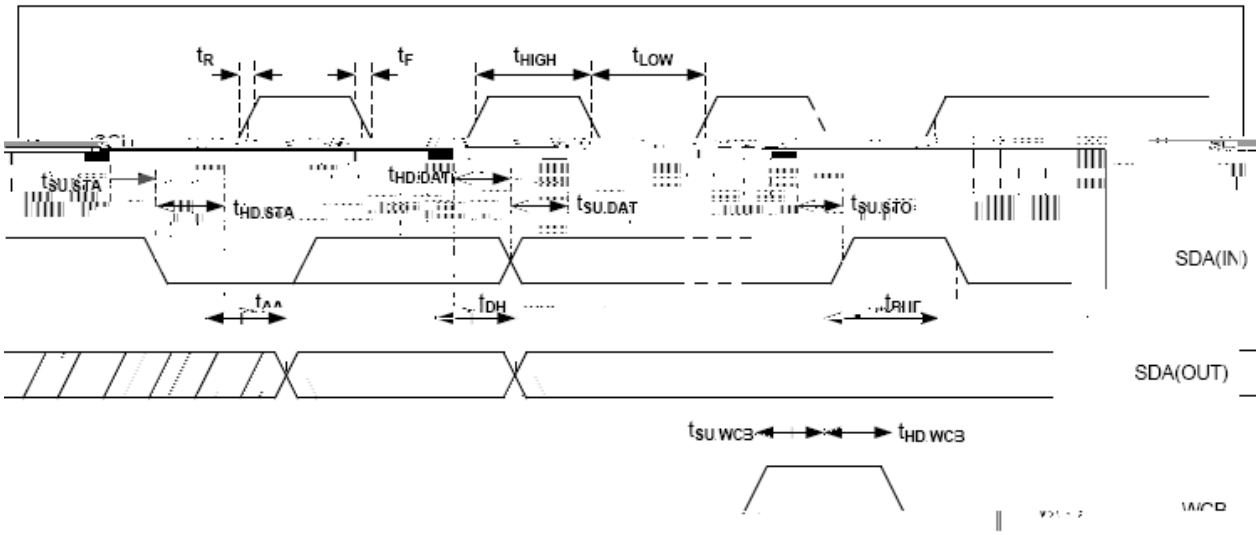
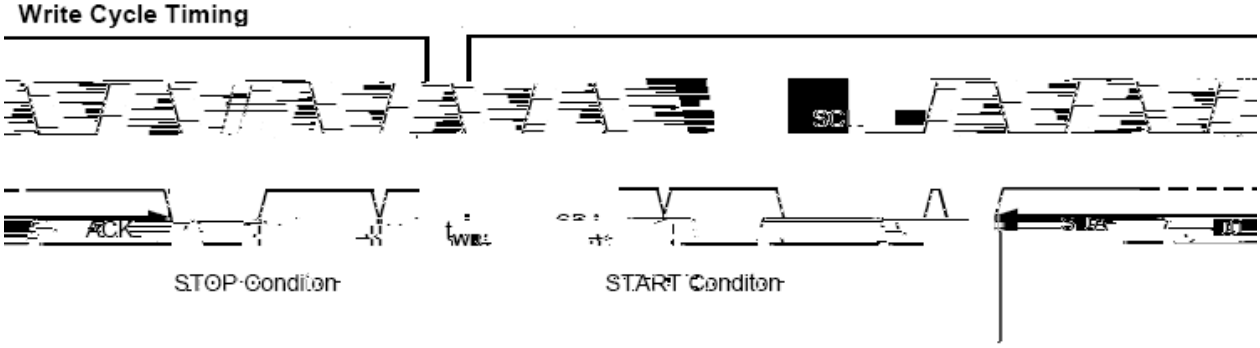


Figure 11 Sequential Read

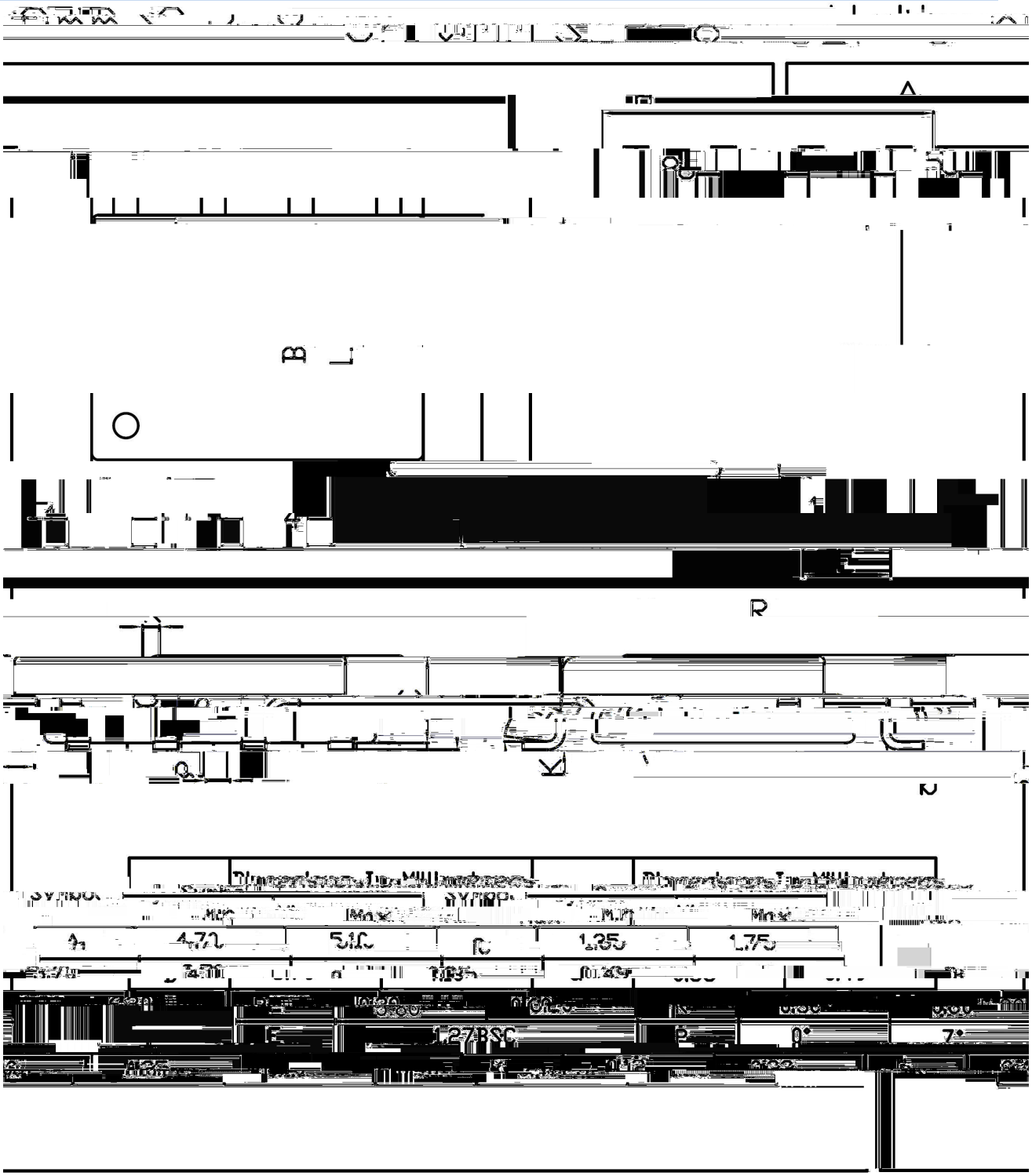
Bus Timing

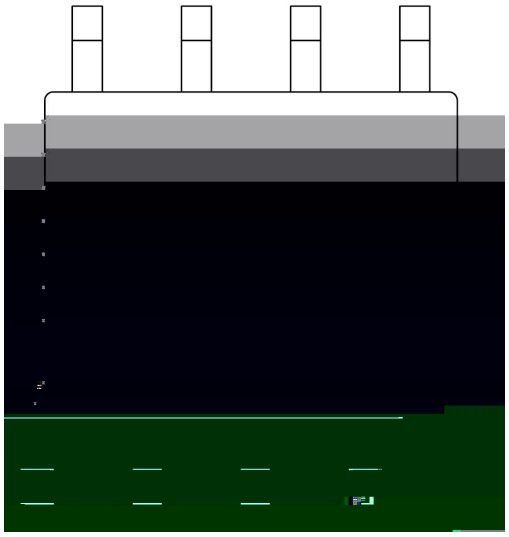


Write Cycle Timing



t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle. Note: The write cycle time


A
B
R
SYMBOL
Min
Max
4.72
5.10
1.35
1.75
1.27BSC
0°
7°



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Note:

BR: Company Code.